

What is claimed is:

1. A system for integrated circuit (IC) design comprising:
at least one structural multi-project wafer (SMPW) comprising a plurality of pre-manufactured and pre-validated functional blocks; and
a streamlined IC design flow incorporating the SMPW and having no IP integration or floor planning requirements.
2. The system of claim 1, wherein the functional blocks of the SMPW comprise structural arrays.
3. The system of claim 1, wherein the SMPW is pre-fabricated up to a contact layer so that a user can customize and program different blocks of the SMPW to the user's requirements.
4. The system of claim 1, wherein the IC design flow has a cycle time of approximately 1-3 months.
5. The system of claim 1, wherein the functional blocks are chosen from a group comprising: metal programmable PLLs; master/slave DLLs; metal programmable I/O elements; sea of gates; memory; and high speed serial links.

6. A component architecture for use in a streamlined integrated circuit (IC) design process comprising:

a plurality of sub-blocks targeted to specific applications, wherein the architecture is pre-fabricated up to a contact layer in order to allow a user to customize and program the sub-blocks to the user's requirements through metallization.

7. The component architecture of claim 6, wherein the sub-blocks are structural arrays.

8. The component architecture of claim 6, wherein the sub-blocks are chosen from a group comprising: metal programmable PLLs; master/slave DLLs; metal programmable I/O elements; sea of gates; memory; and high speed serial links

9. A method for designing an integrated circuit (IC) comprising:
providing a plurality of structural multi-project wafers (SMPWs), each SMPW comprising a plurality of pre-manufactured and pre-validated functional blocks;

if one of the plurality of SMPWs meets an IC designer's requirements, proceeding to a streamlined design flow and production;

if one of the plurality of SMPWs is usable as an intermediate step, extracting usable SMPW component(s) for use in a normal COT flow; and

if one of the plurality of SMPWs does not meet a user's requirement and is not usable as an intermediate step, extracting any usable IP from the plurality of SMPWs for use in a normal COT flow.

10. The method of claim 9, wherein the streamlined design flow has a cycle time of 1-3 months and wherein the normal COT design flow has a cycle time of 12-24 months.

11. A method for providing integrated circuit design assistance comprising:
maintaining an inventory of structural multi-project wafers (SMPWs), each SMPW comprising a plurality of pre-manufactured and pre-validated functional blocks.

12. A method as claimed in claim 11, wherein the functional blocks are metal programmable to a user's specific requirements.

13. A method as claimed in claim 11, further comprising:
determining whether one of the inventory of SMPWs can meet all of a user's IC design requirements or can serve an intermediate step in a user's IC design process, such as market/concept validation or IP validation.

14. A method as claimed in claim 13, further comprising:

determining whether any IP useful to a user's requirement is contained within the inventory of SMPWs.

15. A method as claimed in claim 11, and further comprising:
reducing manufacturing costs to users by sharing the SMPWs among multiple users.

16. A method as claimed in claim 11, and further comprising:
maintaining a pool of validated IP that is embodied in the inventory of SMPWs.

17. A method as claimed in claim 16, and further comprising:
transferring an IP component from the pool of validated IP to programmable logic for use in COT flow.

18. A method as claimed in claim 11, and further comprising:
facilitating migration to a COT flow with the inventory of SMPWs.

19. A method as claimed in claim 11, and further comprising:
providing multiple packaging and assembly options for SMPW users.

20. A method as claimed in claim 19, wherein the packaging and assembly options are chosen from a group comprising: wire bond, flip chip, BGA, plastics and ceramics.